DATA SHEET

74HC4052; 74HCT4052
Dual 4-channel analog multiplexer, demultiplexer

Product specification
2004 Nov 11
Supersedes data of 2003 May 16

Philips
Semiconductors

PHILIPS

Dual 4-channel analog multiplexer, demultiplexer

74HC4052; 74HCT4052

FEATURES

- Wide analog input voltage range from –5 V to +5 V
- Low ON-resistance:
  - 80 Ω (typical) at $V_{CC} - V_{EE}$ = 4.5 V
  - 70 Ω (typical) at $V_{CC} - V_{EE}$ = 6.0 V
  - 60 Ω (typical) at $V_{CC} - V_{EE}$ = 9.0 V
- Logic level translation: to enable 5 V logic to communicate with ±5 V analog signals
- Typical “break before make” built in
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating.

DESCRIPTION

The 74HC4052 and 74HCT4052 are high-speed Si-gate CMOS devices and are pin compatible with the HEF4052B. They are specified in compliance with JEDEC standard no. 7A.

The 74HC4052 and 74HCT4052 are dual 4-channel analog multiplexers or demultiplexers with common select logic. Each multiplexer has four independent inputs/outputs (pins nY0 to nY3) and a common input/output (pin nZ). The common channel select logics include two digital select inputs (pins S0 and S1) and an active LOW enable input (pin $\overline{E}$). When pin $\overline{E}$ = LOW, one of the four switches is selected (low-impedance ON-state) with pins S0 and S1. When pin $\overline{E}$ = HIGH, all switches are in the high-impedance OFF-state, independent of pins S0 and S1.

V_{CC} and GND are the supply voltage pins for the digital control inputs (pins S0, S1, and $\overline{E}$). The V_{CC} to GND ranges are 2.0 V to 10.0 V for 74HC4052 and 4.5 V to 5.5 V for 74HCT4052. The analog inputs/outputs (pins nY0 to nY3 and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

FUNCTION TABLE

INPUT[1]			CHANNEL BETWEEN
$\overline{E}$	S1	S0	
L	L	L	nY0 and nZ
L	L	H	nY1 and nZ
L	H	L	nY2 and nZ
L	H	H	nY3 and nZ
H	X	X	none

Note

1. H = HIGH voltage level
   L = LOW voltage level
   X = don’t care.

QUICK REFERENCE DATA

V_{EE} = GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			74HC4052	74HCT4052	
t_{PZH}/t_{PZL}	turn-on time $\overline{E}$ or Sn to V_{os}	C_L = 15 pF; R_L = 1 kΩ; V_{CC} = 5 V	28	18	ns
t_{PHZ}/t_{PLZ}	turn-off time $\overline{E}$ or Sn to V_{os}	C_L = 15 pF; R_L = 1 kΩ; V_{CC} = 5 V	21	13	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	57	57	pF
C_S	maximum switch capacitance	independent (Y)	5	5	pF
		common (Z)	12	12	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma[(C_L + C_S) \times V_{CC}^2 \times f_o]$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   C_S = maximum switch capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = number of inputs switching;
   $\Sigma[(C_L + C_S) \times V_{CC}^2 \times f_o]$ = sum of the outputs.
2. For 74HC4052 the condition is V_I = GND to V_{CC}
   For 74HCT4052 the condition is V_I = GND to V_{CC} – 1.5 V.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74HC4052D	–40 °C to +125 °C	16	SO16	plastic	SOT109-3
74HCT4052D	–40 °C to +125 °C	16	SO16	plastic	SOT109-3
74HC4052DB	–40 °C to +125 °C	16	SSOP16	plastic	SOT338-1
74HCT4052DB	–40 °C to +125 °C	16	SSOP16	plastic	SOT338-1
74HC4052N	–40 °C to +125 °C	16	DIP16	plastic	SOT38-9
74HCT4052N	–40 °C to +125 °C	16	DIP16	plastic	SOT38-9
74HC4052PW	–40 °C to +125 °C	16	TSSOP16	plastic	SOT403-1
74HC4052BQ	–40 °C to +125 °C	16	DHVQFN16	plastic	SOT763-1
74HCT4052BQ	–40 °C to +125 °C	16	DHVQFN16	plastic	SOT763-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	2Y0	independent input or output
2	2Y2	independent input or output
3	2Z	common input or output
4	2Y3	independent input or output
5	2Y1	independent input or output
6	$\overline{E}$	enable input (active LOW)
7	V_{EE}	negative supply voltage
8	GND	ground (0 V)
9	S1	select logic input
10	S0	select logic input
11	1Y3	independent input or output
12	1Y0	independent input or output
13	1Z	common input or output
14	1Y1	independent input or output
15	1Y2	independent input or output
16	V_{CC}	positive supply voltage

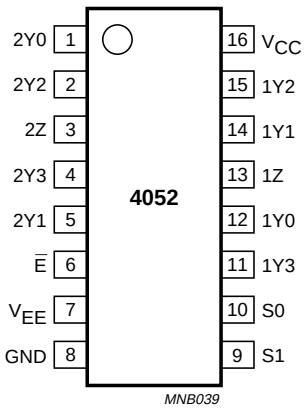
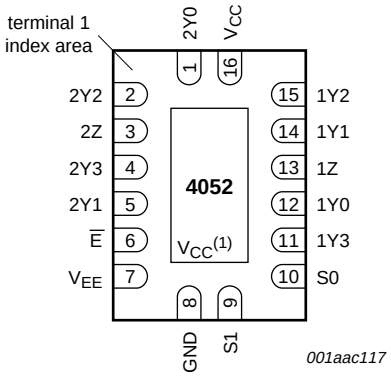


Fig.1 Pin configuration DIP16, SO16 and (T)SSOP16.



Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN16.

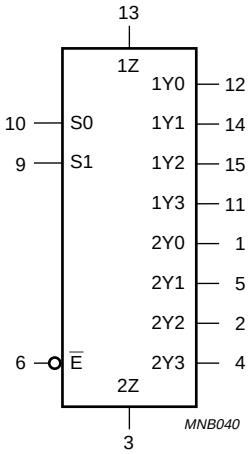


Fig.3 Logic symbol.

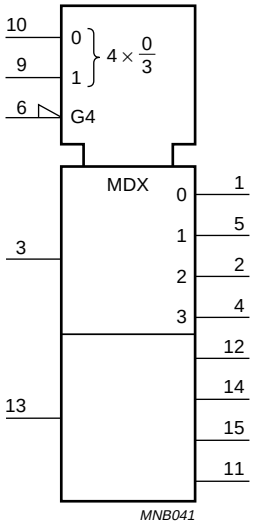


Fig.4 IEC logic symbol.

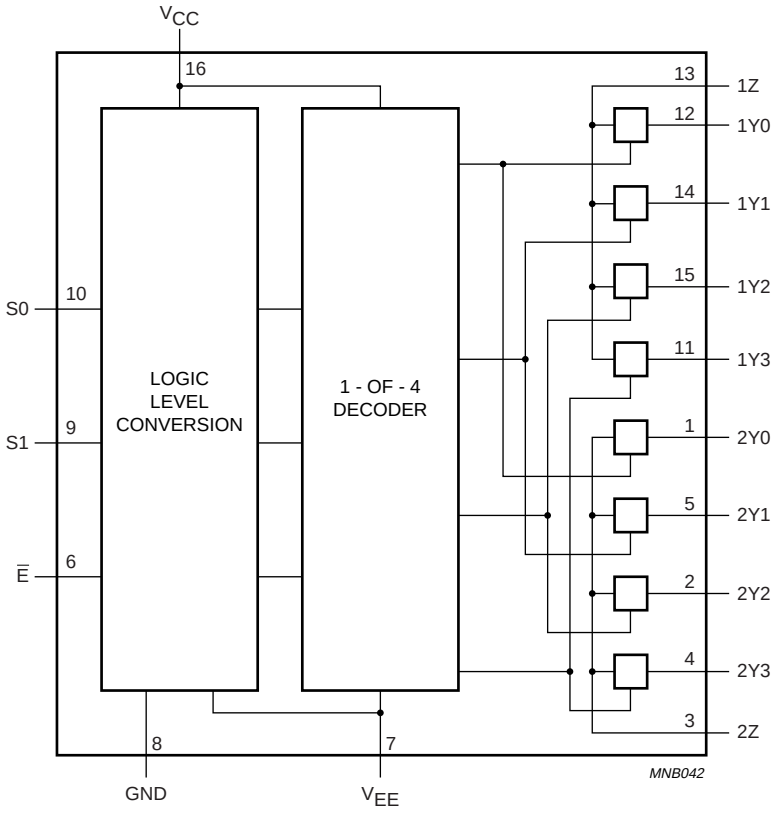


Fig.5 Functional diagram.

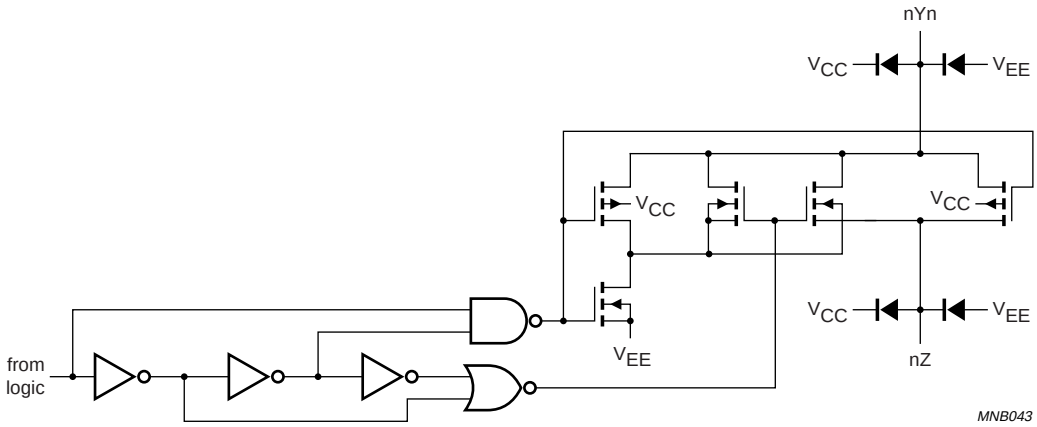


Fig.6 Schematic diagram (one switch).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to V_{EE} = GND (ground = 0 V); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+11.0	V
I_{IK}	input diode current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	–	±20	mA
I_{SK}	switch diode current	$V_S < –0.5$ V or $V_S > V_{CC} + 0.5$ V	–	±20	mA
I_S	switch current	$–0.5 \text{ V} < V_S < V_{CC} + 0.5$ V	–	±25	mA
I_{EE}	V_{EE} current		–	±20	mA
I_{CC}; I_{GND}	V_{CC} or GND current		–	±50	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C; note	–	500	mW
P_S	power dissipation per switch		–	100	mW

Notes

1. To avoid drawing V_{CC} current out of pins nZ, when switch current flows in pins nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into pins nZ, no V_{CC} current will flow out of pins nYn. In this case there is no limit for the voltage drop across the switch, but the voltages at pins nYn and nZ may not exceed V_{CC} or V_{EE}.
2. For DIP16 packages: above 70 °C derate linearly with 12 mW/K.

   For SO16 packages: above 70 °C derate linearly with 8 mW/K.

   For SSOP16 and TSSOP16 packages: above 60 °C derate linearly with 5.5 mW/K.

   For DHVQFN16 packages: above 60 °C derate linearly with 4.5 mW/K.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC4052			74HCT4052			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage	see Figs 7 and 8							
		V_{CC} – GND	2.0	5.0	10.0	4.5	5.0	5.5	V
		V_{CC} – V_{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V
V_I	input voltage		GND	–	V_{CC}	GND	–	V_{CC}	V
V_S	switch voltage		V_{EE}	–	V_{CC}	V_{EE}	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+85	–40	+25	+85	°C
			–40	–	+125	–40	–	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 2.0 V	–	6.0	1000	–	6.0	500	ns
		V_{CC} = 4.5 V	–	6.0	500	–	6.0	500	ns
		V_{CC} = 6.0 V	–	6.0	400	–	6.0	500	ns
		V_{CC} = 10.0 V	–	6.0	250	–	6.0	500	ns

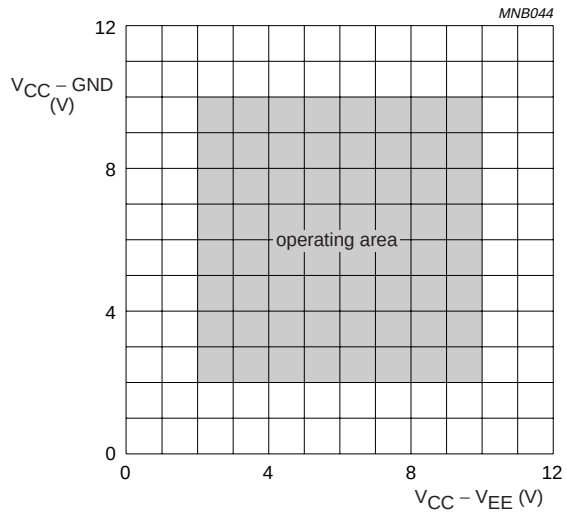


Fig.7 Guaranteed operating area as a function of the supply voltages for 74HC4052.

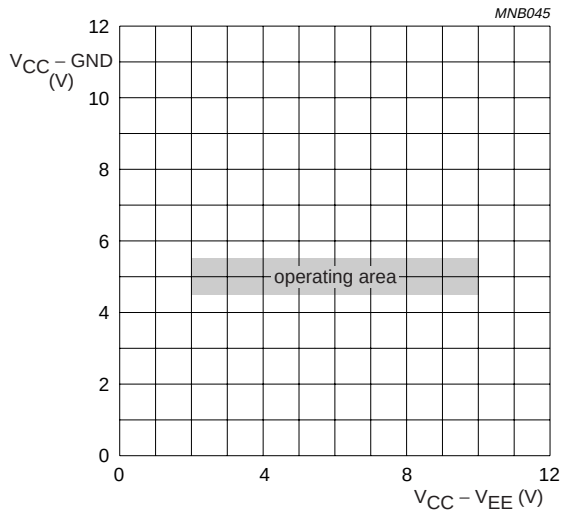


Fig.8 Guaranteed operating area as a function of the supply voltages for 74HCT4052.

DC CHARACTERISTICS

Family 74HC4052

V_{is} is the input voltage at pins nYn or nZ, whichever is assigned as an input; V_{os} is the output voltage at pins nZ or nYn, whichever is assigned as an output; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)	V_{EE} (V)				
T_{amb} = −40 °C to +85 °C; note 1								
V_{IH}	HIGH-level input voltage		2.0	–	1.5	1.2	–	V
			4.5	–	3.15	2.4	–	V
			6.0	–	4.2	3.2	–	V
			9.0	–	6.3	4.7	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.8	0.5	V
			4.5	–	–	2.1	1.35	V
			6.0	–	–	2.8	1.8	V
			9.0	–	–	4.3	2.7	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	6.0	0	–	–	±1.0	μA
			10.0	0	–	–	±2.0	μA
$I_{S(OFF)}$	analog switch OFF-state current	$V_I = V_{IH}$ or V_{IL}; $\|V_S\| = V_{CC} - V_{EE}$; see Fig.9						
		per channel	10.0	0	–	–	±1.0	μA
		all channels	10.0	0	–	–	±2.0	μA
$I_{S(ON)}$	analog switch ON-state current	$V_I = V_{IH}$ or V_{IL}; $\|V_S\| = V_{CC} - V_{EE}$; see Fig.10	10.0	0	–	–	±2.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $V_{is} = V_{EE}$ or V_{CC}; $V_{os} = V_{CC}$ or V_{EE}	6.0	0	–	–	80.0	μA
			10.0	0	–	–	160.0	μA

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)	V_{EE} (V)				
T_{amb} = −40 °C to +125 °C								
V_{IH}	HIGH-level input voltage		2.0	–	1.5	–	–	V
			4.5	–	3.15	–	–	V
			6.0	–	4.2	–	–	V
			9.0	–	6.3	–	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	–	0.5	V
			4.5	–	–	–	1.35	V
			6.0	–	–	–	1.8	V
			9.0	–	–	–	2.7	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	6.0	0	–	–	±1.0	μA
			10.0	0	–	–	±2.0	μA
$I_{S(OFF)}$	analog switch OFF-state current	V_I = V_{IH} or V_{IL}; $\|V_S\|$ = V_{CC} − V_{EE}; see Fig.9						
		per channel	10.0	0	–	–	±1.0	μA
		all channels	10.0	0	–	–	±2.0	μA
$I_{S(ON)}$	analog switch ON-state current	V_I = V_{IH} or V_{IL}; $\|V_S\|$ = V_{CC} − V_{EE}; see Fig.10	10.0	0	–	–	±2.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}	6.0	0	–	–	160	μA
			10.0	0	–	–	320.0	μA

Note

1. All typical values are measured at T_{amb} = 25 °C.

Family 74HCT4052

V_{is} is the input voltage at pins nYn or nZ, whichever is assigned as an input; V_{os} is the output voltage at pins nZ or nYn, whichever is assigned as an output; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)	V_{EE} (V)				
T_{amb} = −40 °C to +85 °C; note 1								
V_{IH}	HIGH-level input voltage		4.5 to 5.5	–	2.0	1.6	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	1.2	0.8	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	5.5	0	–	–	±1.0	μA
$I_{S(OFF)}$	analog switch OFF-state current	$V_I = V_{IH}$ or V_{IL}; $\lvert V_S \rvert = V_{CC} - V_{EE}$; see Fig.9						
		per channel	10.0	0	–	–	±1.0	μA
		all channels	10.0	0	–	–	±2.0	μA
$I_{S(ON)}$	analog switch ON-state current	$V_I = V_{IH}$ or V_{IL}; $\lvert V_S \rvert = V_{CC} - V_{EE}$; see Fig.10	10.0	0	–	–	±2.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $V_{is} = V_{EE}$ or V_{CC}; $V_{os} = V_{CC}$ or V_{EE}	5.5	0	–	–	80.0	μA
			5.0	–5.0	–	–	160.0	μA
ΔI_{CC}	additional quiescent supply current per input	$V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND	4.5 to 5.5	0	–	45	202.5	μA
T_{amb} = −40 °C to +125 °C								
V_{IH}	HIGH-level input voltage		4.5 to 5.5	–	2.0	–	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	–	0.8	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	5.5	0	–	–	±1.0	μA
$I_{S(OFF)}$	analog switch OFF-state current	$V_I = V_{IH}$ or V_{IL}; $\lvert V_S \rvert = V_{CC} - V_{EE}$; see Fig.9						
		per channel	10.0	0	–	–	±1.0	μA
		all channels	10.0	0	–	–	±2.0	μA
$I_{S(ON)}$	analog switch ON-state current	$V_I = V_{IH}$ or V_{IL}; $\lvert V_S \rvert = V_{CC} - V_{EE}$; see Fig.10	10.0	0	–	–	±2.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $V_{is} = V_{EE}$ or V_{CC}; $V_{os} = V_{CC}$ or V_{EE}	5.5	0	–	–	160.0	μA
			5.0	–5.0	–	–	320.0	μA
ΔI_{CC}	additional quiescent supply current per input	$V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND	4.5 to 5.5	0	–	–	220.5	μA

Note

1. All typical values are measured at T_{amb} = 25 °C.

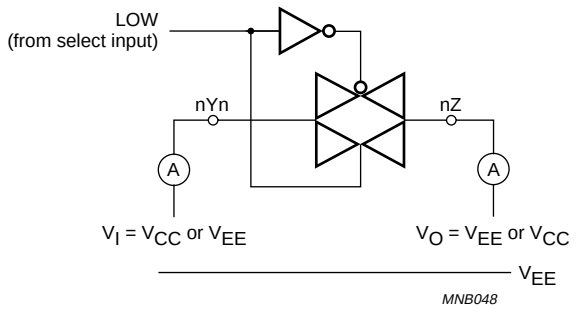


Fig.9 Test circuit for measuring OFF-state current.

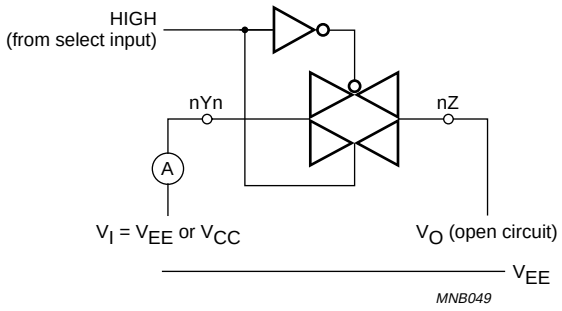


Fig.10 Test circuit for measuring ON-state current.

Resistance R_{ON} for 74HC4052 and 74HCT4052

V_{is} is the input voltage at pins nYn or nZ, whichever is assigned as an input; see notes 1 and 2; see Fig.11.

SYMBOL	PARAMETER	TEST CONDITIONS				MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)	V_{EE} (V)	I_S (μA)				
T_{amb} = −40 °C to +85 °C; note 3									
$R_{ON(peak)}$	ON-resistance (peak)	V_{is} = V_{CC} to V_{EE}; V_I = V_{IH} or V_{IL}	2.0	0	100	–	–	–	Ω
			4.5	0	1000	–	100	225	Ω
			6.0	0	1000	–	90	200	Ω
			4.5	–4.5	1000	–	70	165	Ω
$R_{ON(rail)}$	ON-resistance (rail)	V_{is} = V_{EE}; V_I = V_{IH} or V_{IL}	2.0	0	100	–	150	–	Ω
			4.5	0	1000	–	80	175	Ω
			6.0	0	1000	–	70	150	Ω
			4.5	–4.5	1000	–	60	130	Ω
		V_{is} = V_{CC}; V_I = V_{IH} or V_{IL}	2.0	0	100	–	150	–	Ω
			4.5	0	1000	–	90	200	Ω
			6.0	0	1000	–	80	175	Ω
			4.5	–4.5	1000	–	65	150	Ω
ΔR_{ON}	maximum ON-resistance difference between any two channels	V_{is} = V_{CC} to V_{EE}; V_I = V_{IH} or V_{IL}	2.0	0	–	–	–	–	Ω
			4.5	0	–	–	9	–	Ω
			6.0	0	–	–	8	–	Ω
			4.5	–4.5	–	–	6	–	Ω
T_{amb} = −40 °C to +125 °C									
$R_{ON(peak)}$	ON-resistance (peak)	V_{is} = V_{CC} to V_{EE}; V_I = V_{IH} or V_{IL}	2.0	0	100	–	–	–	Ω
			4.5	0	1000	–	–	270	Ω
			6.0	0	1000	–	–	240	Ω
			4.5	–4.5	1000	–	–	195	Ω
$R_{ON(rail)}$	ON-resistance (rail)	V_{is} = V_{EE}; V_I = V_{IH} or V_{IL}	2.0	0	100	–	–	–	Ω
			4.5	0	1000	–	–	210	Ω
			6.0	0	1000	–	–	180	Ω
			4.5	–4.5	1000	–	–	160	Ω
		V_{is} = V_{CC}; V_I = V_{IH} or V_{IL}	2.0	0	100	–	–	–	Ω
			4.5	0	1000	–	–	240	Ω
			6.0	0	1000	–	–	210	Ω
			4.5	–4.5	1000	–	–	180	Ω

Notes

1. For 74HC4052: V_{CC} – GND or V_{CC} – V_{EE} = 2.0, 4.5, 6.0 and 9.0 V; for 74HCT4052: V_{CC} – GND = 4.5 and 5.5 V, V_{CC} – V_{EE} = 2.0, 4.5, 6.0 and 9.0 V.
2. When supply voltages (V_{CC} – V_{EE}) near 2.0 V the analog switch ON-resistance becomes extremely non-linear. When using a supply of 2 V, it is recommended to use these devices only for transmitting digital signals.
3. All typical values are measured at T_{amb} = 25 °C.

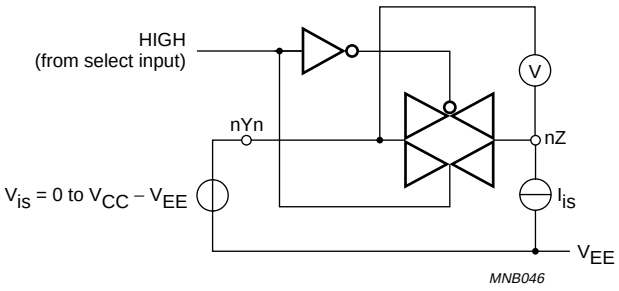
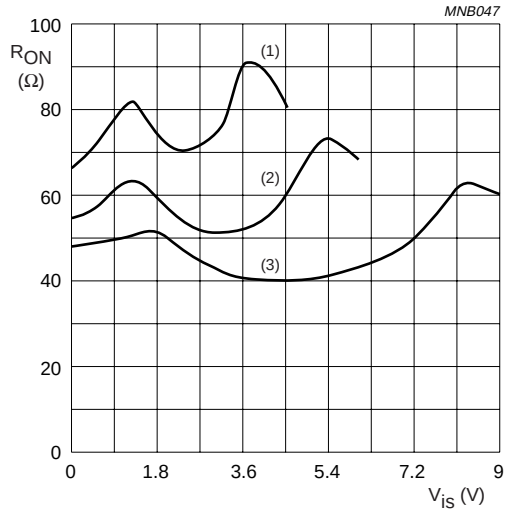


Fig.11 Test circuit for measuring R_{ON}.



V_{is} = 0 V to $V_{CC} - V_{EE}$
(1) V_{CC} = 4.5 V
(2) V_{CC} = 6 V
(3) V_{CC} = 9 V

Fig.12 Typical R_{ON} as a function of input voltage V_{is}.

AC CHARACTERISTICS

Type 74HC4052

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)	V_{EE} (V)				
T_{amb} = −40 °C to +85 °C; note 1								
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}	R_L = ∞; see Fig.19	2.0	0	–	14	75	ns
			4.5	0	–	5	15	ns
			6.0	0	–	4	13	ns
			4.5	–4.5	–	4	10	ns
t_{PZH}/t_{PZL}	turn-on time $\overline{E}$, Sn to V_{os}	R_L = ∞; see Figs 20, 22 and 21	2.0	0	–	105	405	ns
			4.5	0	–	38	81	ns
			6.0	0	–	30	69	ns
			4.5	–4.5	–	26	58	ns
t_{PHZ}/t_{PLZ}	turn-off time $\overline{E}$, Sn to V_{os}	R_L = 1 kΩ; see Figs 20, 22 and 21	2.0	0	–	74	315	ns
			4.5	0	–	27	63	ns
			6.0	0	–	22	54	ns
			4.5	–4.5	–	22	48	ns
T_{amb} = −40 °C to +125 °C								
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}	R_L = ∞; see Fig.19	2.0	0	–	–	90	ns
			4.5	0	–	–	18	ns
			6.0	0	–	–	15	ns
			4.5	–4.5	–	–	12	ns
t_{PZH}/t_{PZL}	turn-on time $\overline{E}$, Sn to V_{os}	R_L = ∞; see Figs 20, 22 and 21	2.0	0	–	–	490	ns
			4.5	0	–	–	98	ns
			6.0	0	–	–	83	ns
			4.5	–4.5	–	–	69	ns
t_{PHZ}/t_{PLZ}	turn-off time $\overline{E}$, Sn to V_{os}	R_L = 1 kΩ; see Figs 20, 22 and 21	2.0	0	–	–	375	ns
			4.5	0	–	–	75	ns
			6.0	0	–	–	64	ns
			4.5	–4.5	–	–	57	ns

Note

1. All typical values are measured at T_{amb} = 25 °C.

Type 74HCT4052

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)	V_{EE} (V)				
T_{amb} = –40 °C to +85 °C; note 1								
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}	R_L = ∞; see Fig.19	4.5	0	–	5	15	ns
			4.5	–4.5	–	4	10	ns
t_{PZH}/t_{PZL}	turn-on time $\overline{E}$, Sn to V_{os}	R_L = 1 kΩ; see Figs 20, 22 and 21	4.5	0	–	41	88	ns
			4.5	–4.5	–	28	60	ns
t_{PHZ} t_{PLZ}	turn-off time $\overline{E}$, Sn to V_{os}	R_L = 1 kΩ; see Figs 20, 22 and 21	4.5	0	–	26	63	ns
			4.5	–4.5	–	21	48	ns
T_{amb} = –40 °C to +125 °C								
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}	R_L = ∞; see Fig.19	4.5	0	–	–	18	ns
			4.5	–4.5	–	–	12	ns
t_{PZH}/t_{PZL}	turn-on time $\overline{E}$, Sn to V_{os}	R_L = 1 kΩ; see Figs 20, 22 and 21	4.5	0	–	–	105	ns
			4.5	–4.5	–	–	72	ns
t_{PHZ}/t_{PLZ}	turn-off time $\overline{E}$, Sn to V_{os}	R_L = 1 kΩ; see Figs 20, 22 and 21	4.5	0	–	–	75	ns
			4.5	–4.5	–	–	57	ns

Note

1. All typical values are measured at T_{amb} = 25 °C.

Type 74HC4052 and 74HCT4052

Recommended conditions and typical values; GND = 0 V; T_{amb} = 25 °C; C_L = 50 pF. V_{is} is the input voltage at pins nYn or nZ, whichever is assigned as an input. V_{os} is the output voltage at pins nYn or nZ, whichever is assigned as an output.

SYMBOL	PARAMETER	TEST CONDITIONS				TYP.	UNIT
		OTHER	$V_{is(p-p)}$ (V)	V_{CC} (V)	V_{EE} (V)		
d_{sin}	sine-wave distortion	f = 1 kHz; R_L = 10 kΩ; see Fig.13	4.0	2.25	–2.25	0.04	%
			8.0	4.5	–4.5	0.02	%
		f = 10 kHz; R_L = 10 kΩ; see Fig.13	4.0	2.25	–2.25	0.12	%
			8.0	4.5	–4.5	0.06	%
$\alpha_{OFF(feedthr)}$	switch OFF signal feed-through	R_L = 600 Ω; f = 1 MHz; see Figs 14 and 15	note 1	2.25	–2.25	–50	dB
				4.5	–4.5	–50	dB
$\alpha_{ct(s)}$	crosstalk between two switches/multiplexers	R_L = 600 Ω; f = 1 MHz; see Fig.16	note 1	2.25	–2.25	–60	dB
				4.5	–4.5	–60	dB
$V_{ct(p-p)}$	crosstalk voltage between control and any switch (peak-to-peak value)	R_L = 600 Ω; f = 1 MHz; $\overline{E}$ or Sn, square-wave between V_{CC} and GND, $t_r = t_f$ = 6 ns; see Fig.17	–	4.5	0	110	mV
				4.5	–4.5	220	mV
f_{max}	minimum frequency response (–3dB)	R_L = 50 Ω; see Figs 13 and 18	note 2	2.25	–2.25	170	MHz
				4.5	–4.5	180	MHz
C_S	maximum switch capacitance	independent (Y)	–	–	–	5	pF
		common (Z)	–	–	–	12	pF

Notes

1. Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

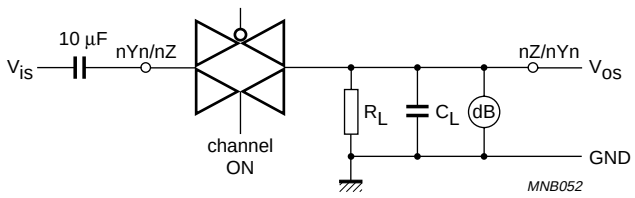


Fig.13 Test circuit for measuring sine-wave distortion and minimum frequency response.

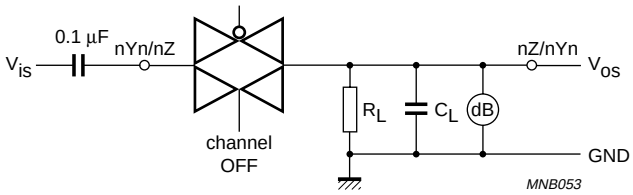
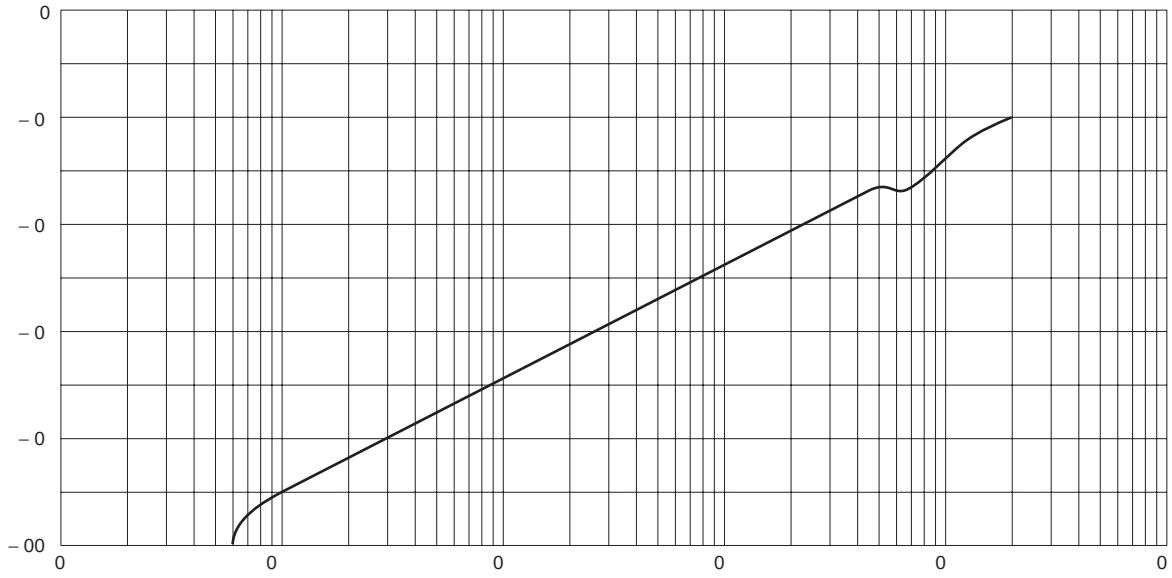
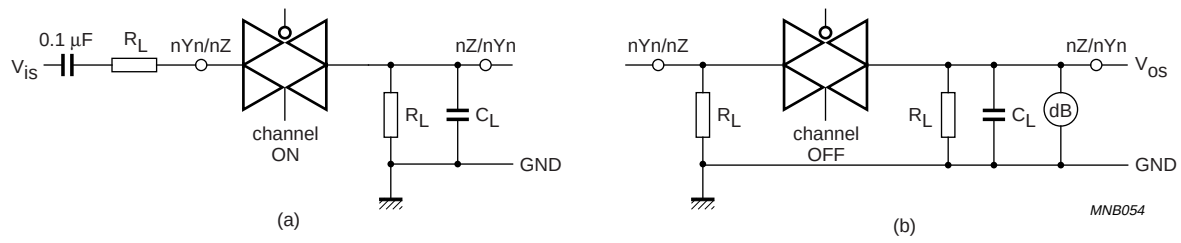


Fig.14 Test circuit for measuring switch OFF signal feed-through.



Test conditions: V_{CC} = 4.5 V; GND = 0 V; V_{EE} = –4.5 V; R_L = 50 Ω; R_{source} = 1 kΩ.

Fig.15 Typical switch OFF signal feed-through as a function of frequency.



(a) channel ON condition.

(b) channel OFF condition.

Fig.16 Test circuits for measuring crosstalk between any two switches/multiplexers.

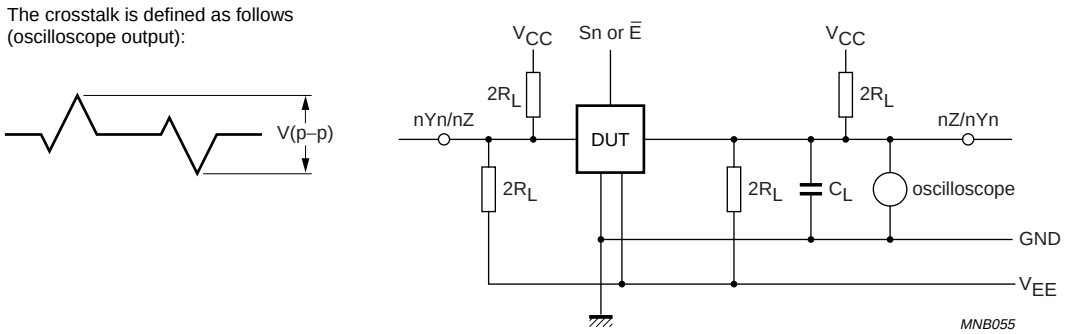
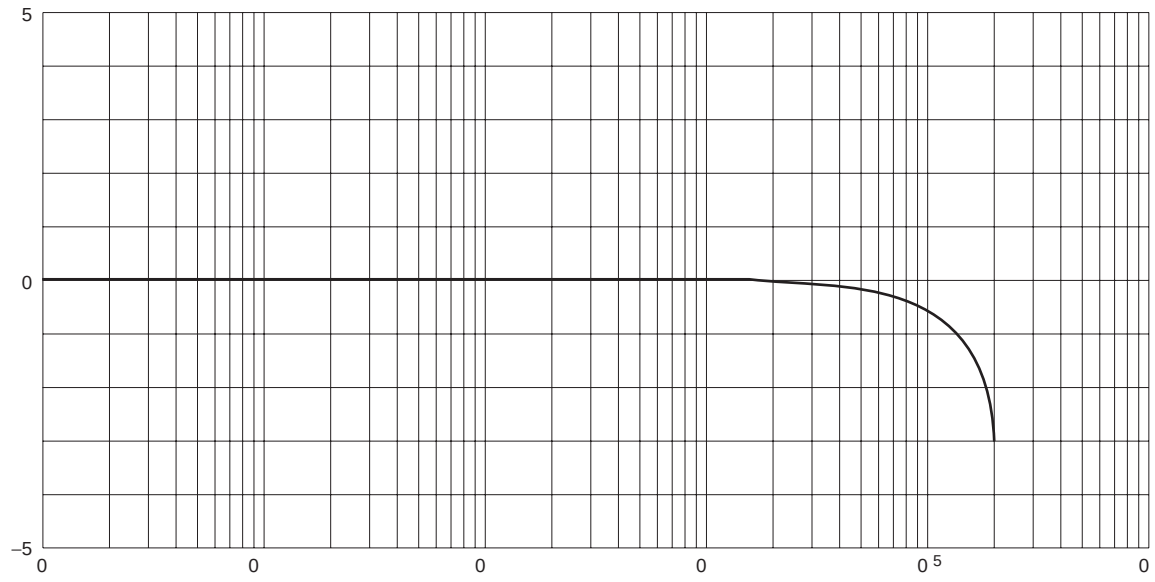


Fig.17 Test circuit for measuring crosstalk between control and any switch.



Test conditions: V_{CC} = 4.5 V; GND = 0 V; V_{EE} = –4.5 V; R_L = 50 Ω; R_{source} = 1 kΩ.

Fig.18 Typical frequency response.

AC WAVEFORMS

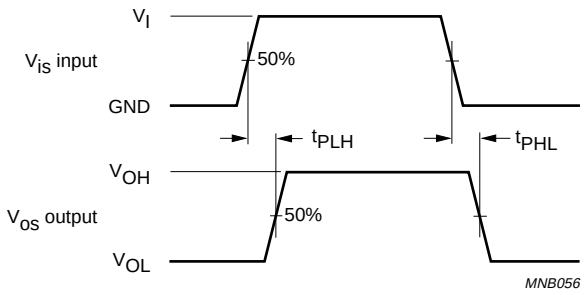
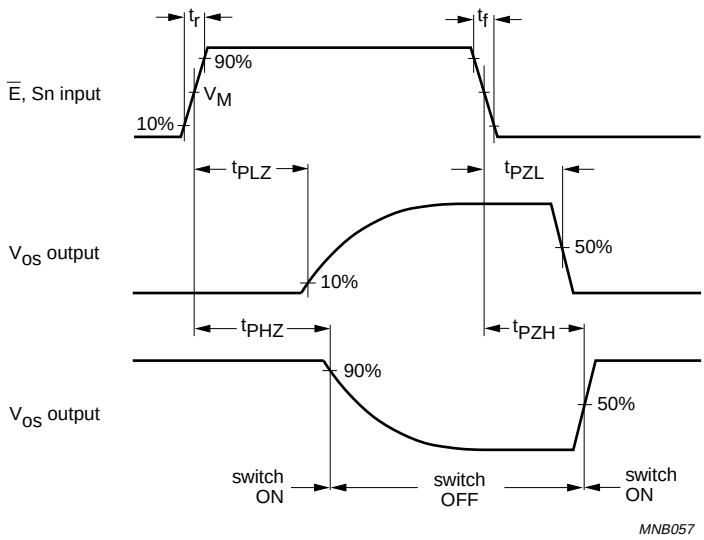
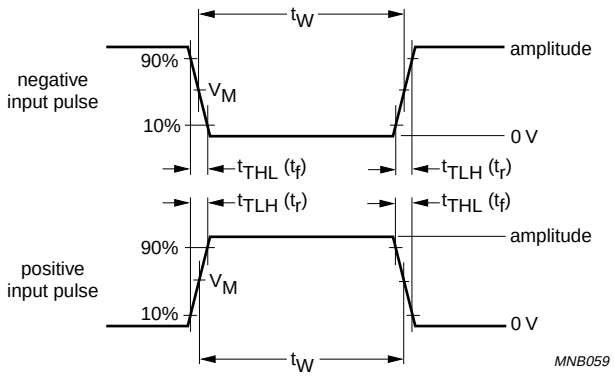


Fig.19 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.



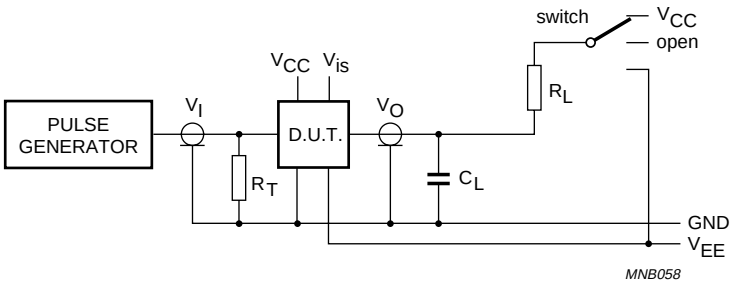
For 74HC4052: V_M = 50 %; V_I = GND to V_{CC}.
For 74HCT4052: V_M = 1.3 V; V_I = GND to 3 V.

Fig.20 Waveforms showing the turn-on and turn-off times.



FAMILY	AMPLITUDE	V_M	t_r and t_f	
			f_{max}; PULSE WIDTH	OTHER
74HC4052	V_{CC}	50 %	< 2 ns	6 ns
74HCT4052	3.0 V	1.3 V	< 2 ns	6 ns

Fig.21 Input pulse definitions.



TEST	SWITCH	V_{is}
t_{PZH}	V_{EE}	V_{CC}
t_{PZL}	V_{CC}	V_{EE}
t_{PHZ}	V_{EE}	V_{CC}
t_{PLZ}	V_{CC}	V_{EE}
other	open	pulse

Definitions for test circuit:

R_L = load resistance

C_L = load capacitance including jig and probe capacitance.

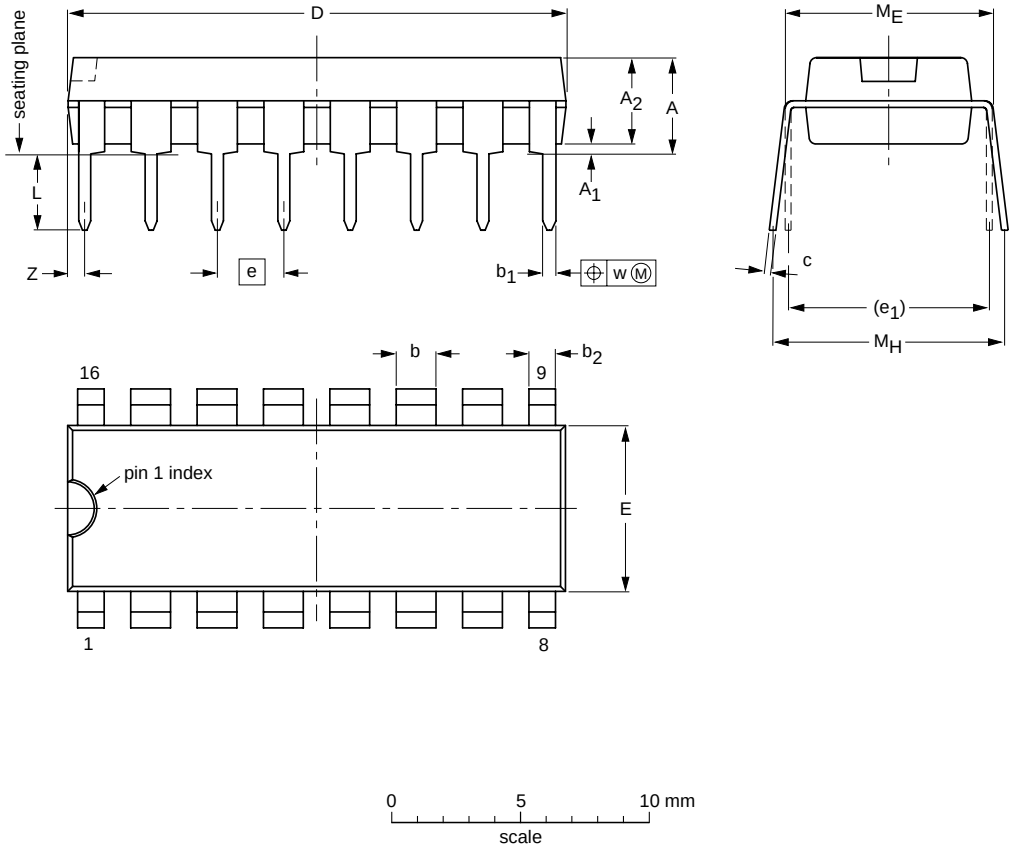
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

$t_r = t_f$ = 6 ns; when measuring f_{max}, there is no constraint to t_r and t_f with 50 % duty factor.

Fig.22 Test circuit for measuring AC performance.

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-9**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

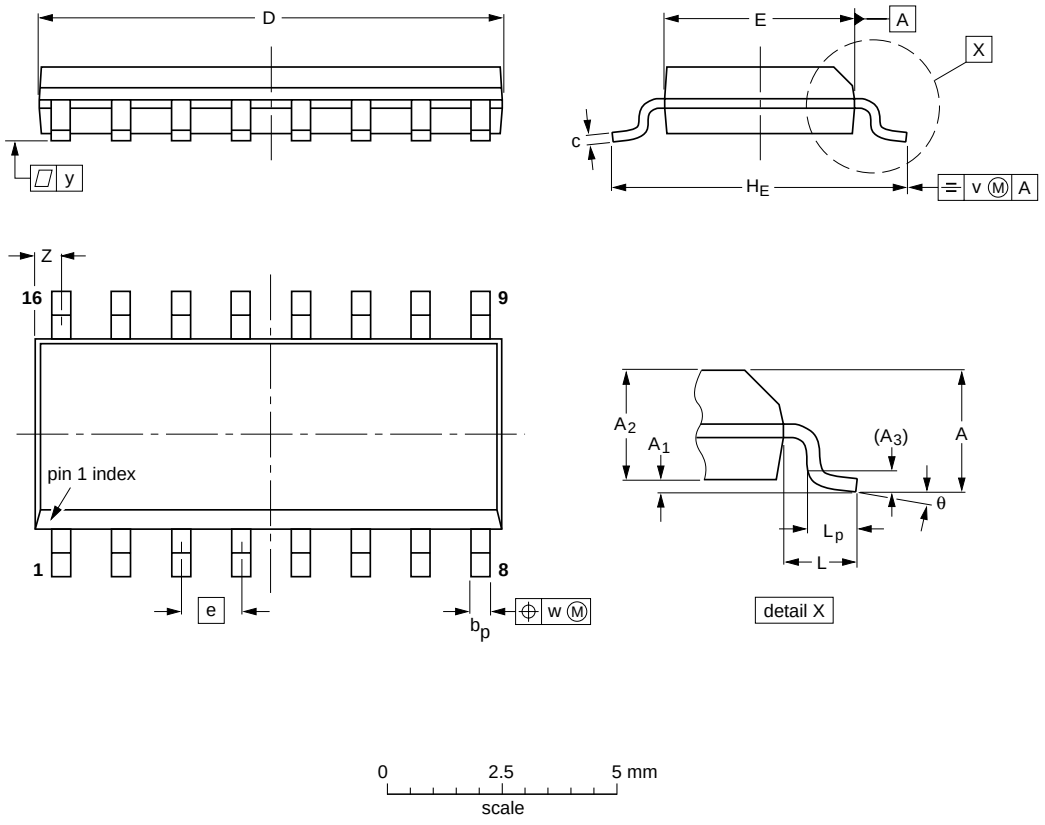
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.32	0.38	3.56	1.65 1.40	0.51 0.41	1.14 0.76	0.36 0.20	19.3 18.8	6.45 6.24	2.54	7.62	3.81 2.92	8.23 7.62	9.40 8.38	0.254	0.76
inches	0.17	0.015	0.14	0.065 0.055	0.020 0.016	0.045 0.030	0.014 0.008	0.76 0.74	0.254 0.246	0.1	0.3	0.150 0.115	0.324 0.300	0.37 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-9						~~97-07-24~~ 03-03-12

SO16: plastic small outline package; 16 leads; body width 3.9 mm; body thickness 1.47 mm **SOT109-3**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

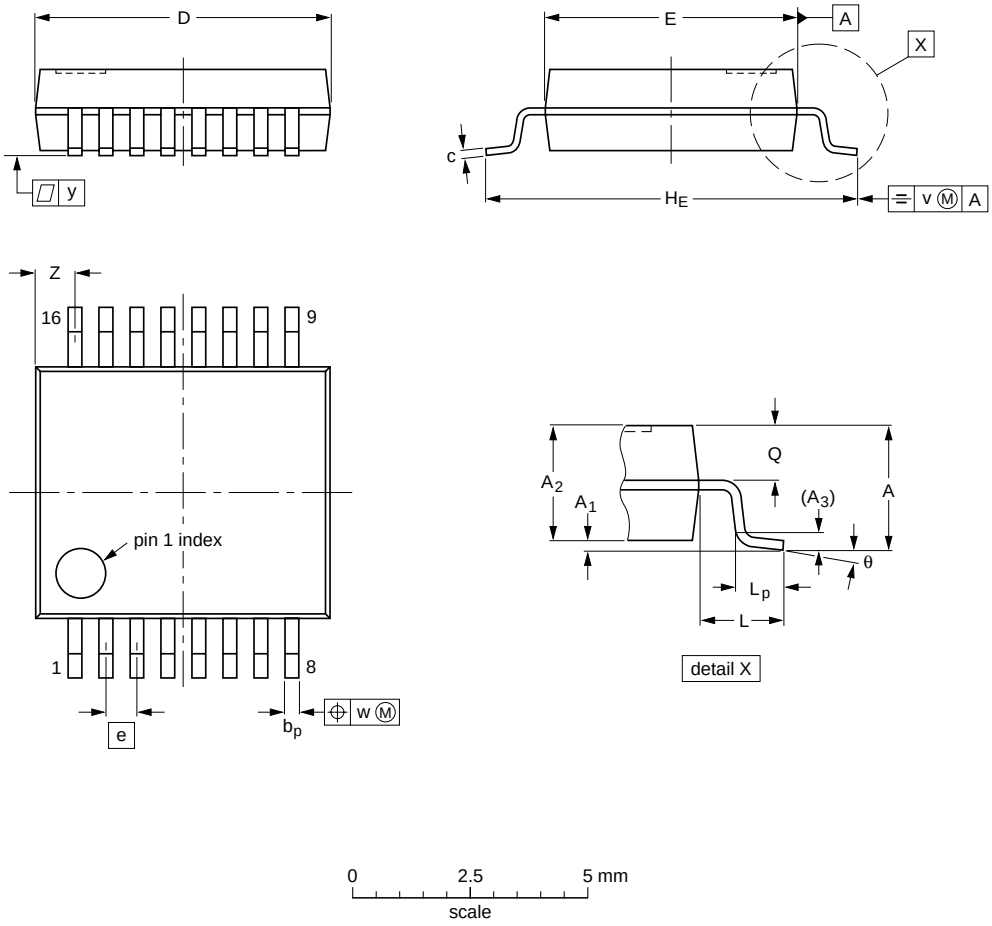
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.55 1.40	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.061 0.055	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-3		MS-012AC				~~98-12-23~~ 03-02-19

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

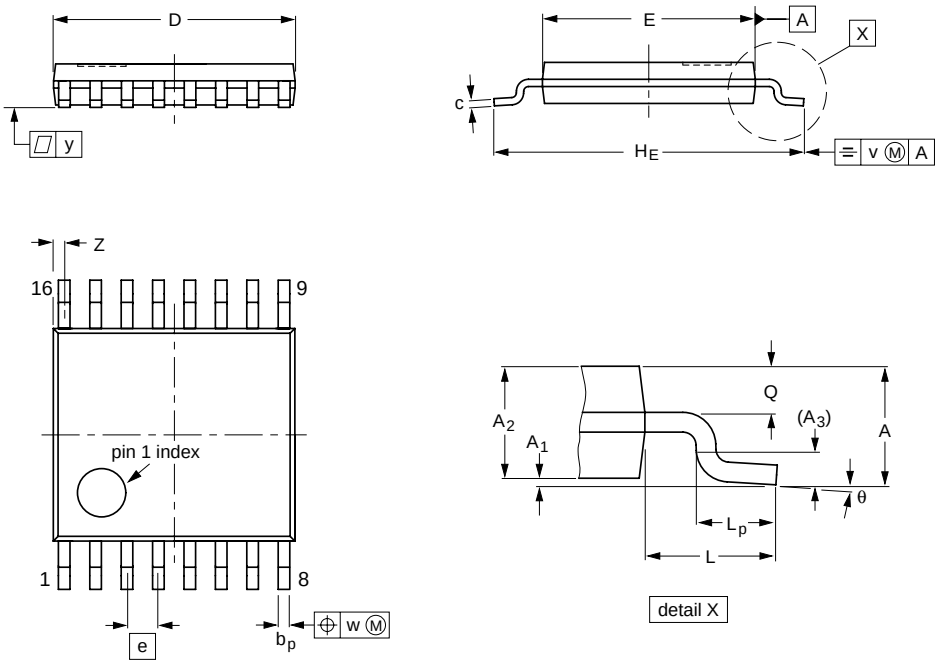
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

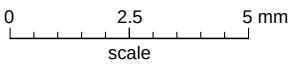
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





DIMENSIONS (mm are the original dimensions)

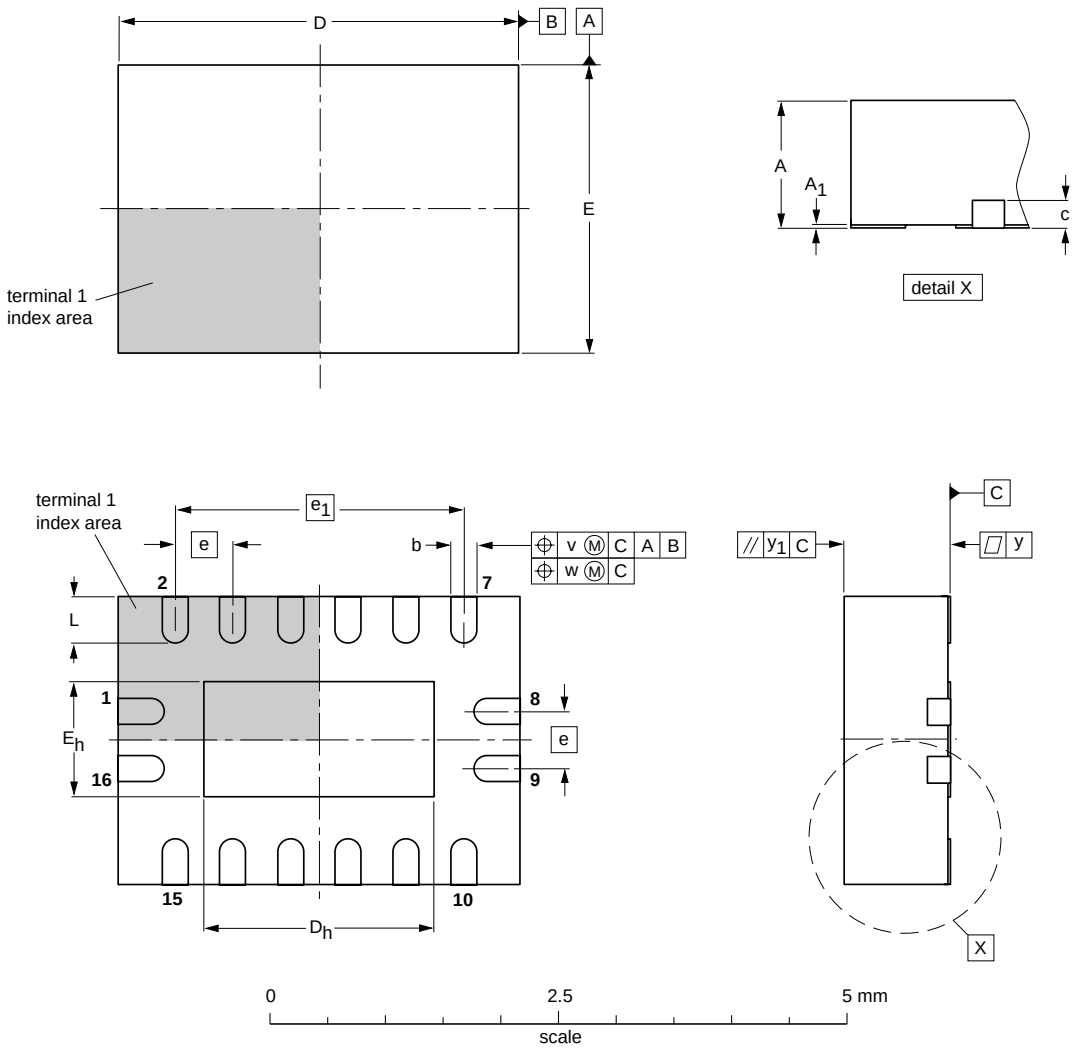
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

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